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Suppressing Hexagonal Defects in Ex Situ Remote Plasma Dry Etch Processing

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***Abstract*—Hexagonal silicon oxide defects induced by an ex-situ remote plasma dry etch pre-clean process (SiCoNi™) were observed at the NPN emitter step of a 40 nm BiCMOS device, leading to high defect density and device yield loss. In this work, a systematic investigation was performed to identify the root cause and formation mechanism of these defects. Comprehensive characterization and experiments reveal that fluorosilicate byproducts trapped in the frontside silicon nitride layer interact with moisture absorbed in the backside TEOS-based silicon oxide during FOUP storage, leading to localized silicon oxide crystallization. Although aggressive annealing can eliminate the defects, it deteriorates the doping profile and device performance. In contrast, removal of the wafer backside TEOS layer effectively suppresses defect formation without compromising device performance. This study provides practical insights into SiCoNi-induced defect formation and proposes compatible mitigation strategies for remote plasma-assisted dry clean processes in advanced technologies.**

***Index Terms*—Heterojunction bipolar transistor, defect density, interface, process integration, SiCoNi™ cleaning**

I. INTRODUCTION

IN the semiconductor industry, the continuous scaling of transistor components and the integration of heterogeneous devices on a single platform have enabled improved device performance while reducing fabrication costs. Among these platforms, BiCMOS technology combines the high-speed capability of bipolar transistors with the low-power consumption of complementary metal-oxide-semiconductor (CMOS) devices. Modern heterojunction bipolar transistors (HBTs) rely on epitaxial growth to form the collector, base, and emitter layers with in-situ doping. This approach enables precise control of dopant concentration and profiles, thereby improving device performance. However, epitaxial growth requires a low-oxygen surface prior to each layer process, while maintaining a low thermal budget to minimize dopant redistribution and preserve the intended doping profile. Consequently, the pre-clean process prior to each epitaxial layer formation has become a critical step that directly impacts epitaxial quality and overall device performance.

Conventionally, various wet chemical methods have been employed for pre-clean processes. Single-step HF or HCl dip cleaning requires stringent queue-time control to minimize silicon surface re-oxidation. In addition, these methods often suffer from high residual oxygen content, isotropic etching behavior, poor oxide selectivity, and increased defect density [1]-[5]. RCA and other wet chemical cleaning processes can improve defect density and eliminate foreign contaminants. However, they inevitably lead to the formation of chemical oxides with varying thicknesses, which may cause dopant trapping at the interface and hinder the subsequent epitaxy process [6]-[8]. Alternatively, in-situ high-temperature hydrogen bake is commonly employed in epitaxial processes to remove surface oxides. Nevertheless, the additional thermal budget can induce dopant redistribution, which is detrimental to device performance [7]-[9].

Over the past decade, a remote plasma dry chemical cleaning technology, known as the SiCoNi™ process, has been developed and increasingly adopted in advanced semiconductor manufacturing, spanning technology nodes from 65 nm to 14 nm [2], [10]. The SiCoNi process employs a plasma-assisted etch mechanism, in which a surface oxide layer is chemically converted into a solid $(NH_4)_2SiF_6$ salt and subsequently removed through low-temperature thermal sublimation. The SiCoNi process has been widely implemented as a pre-clean step for silicidation processes involving Ni, Co, and Ti [1], [2], [11], [12], as well as for middle-of-line (MOL) contact formation and contact glue layer preparation [10], [13]. In addition, the SiCoNi process has been extensively studied as a pre-clean process for epitaxial growth of various materials, including Si, SiGe, SiGeB and GaAs [3], [5], [6], [8], [14]-[16]. Beyond pre-clean applications, the SiCoNi process has also been employed for shallow trench oxide recess and dummy dielectric removal, demonstrating its flexibility across multiple process modules [17]-[20]. The widespread application of the SiCoNi process is attributed to several key advantages, including high selectivity between oxide and other materials [2], [5], [11], [21]-[23], elimination of queue-time dependency [1], [2], and consistent etch rates across different oxide types [21], [24].

Despite these advantages, the SiCoNi process can introduce non-negligible defect issues associated with residual reaction byproducts, which have not been systematically investigated. It is generally assumed that the solid reaction byproduct, $(NH_4)_2SiF_6$, is fully decomposed into volatile species, including SiF_4, NH_3, and HF, at approximately 200 °C in the SiCoNi chamber [3], [25]. However, various studies have reported a higher fluorine concentration detected on wafer surfaces after the SiCoNi cleaning process, nearly four times that observed after conventional HF cleaning [1]-[3], [7], [10], [12], [21], [26]-[28]. This suggests incomplete sublimation and removal of the $(NH_4)_2SiF_6$ byproduct, leading to residual fluorine contamination on the surface. In addition, a single-step SiCoNi clean process has been reported to generate a significantly higher defect density compared with conventional cleaning

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processes [23]. To mitigate these issues, various studies have explored hybrid cleaning schemes combining the SiCoNi process with conventional techniques such as hydrogen bake and wet chemical cleaning [3], [7], [8], [23]. While such approaches can partially alleviate residual fluorine contamination, the integration of wet cleaning steps with the SiCoNi process has been shown to induce high haze levels and surface roughening after re-epitaxy [4]. Moreover, the additional high-temperature hydrogen bake can alter doping profiles, thereby negating the low thermal budget advantage of the SiCoNi process. Thus, these hybrid approaches are incompatible with advanced device integration requirements. Furthermore, the fundamental formation mechanism of SiCoNi process-induced defects remains insufficiently understood, posing risks in terms of inline defectivity, epitaxial quality, and device yield.

Therefore, in this work, we systematically investigate the formation mechanism of SiCoNi process-induced hexagonal defects and develop an effective mitigation strategy to suppress defect formation without compromising process integration or device performance. The findings of this study are not limited to a specific HBT emitter pre-clean process but also provide broader insights into plasma-assisted surface preparation for advanced semiconductor manufacturing.

II. Experimental Setup and Methods

In this study, 300 mm p-type Si (100) blanket test wafers were used as monitor samples. In addition, patterned wafers with 40 nm feature sizes at the emitter layer of a heterojunction bipolar transistor (HBT) device were employed to investigate SiCoNi process-induced hexagonal defects. All wafers were stored in standard 300 mm FOUPs under cleanroom ambient conditions.

The ex-situ SiCoNi process was performed at a chamber pressure of ~10 Torr. NF_3 and NH_3 were introduced as reactive gases, with H_2 serving as the carrier gas. The process consisted of a low temperature etch step with a recipe setpoint of 35 °C for ~10 s, followed by a thermal bake step at 180 °C for ~100 s.

The SiCoNi process is a three-step remote plasma dry etch technique developed to selectively remove silicon dioxide while minimizing interaction with silicon, silicon nitride, and other materials. The overall working principle is schematically illustrated in Fig. 1, and the associated chemical reactions can be represented as follows [8]:

Step 1: Generation of reactive species in a remote plasma cavity

$$NF_3 + 3NH_3 \rightarrow N_2 + NH_4F + NH_4F{\cdot}HF$$

Step 2: Selective chemical reaction with SiO_2 at low temperature (~35 °C)

$$6NH_4F{\cdot}HF + SiO_2 \rightarrow (NH_4)_2SiF_6\ (\text{solid}) + 2H_2O + 4NH_3$$

Step 3: Thermal sublimation of the byproduct (~ 180 °C)

$$(NH_4)_2SiF_6\ (\text{solid}) \rightarrow SiF_4\ (\text{gas}) + 2NH_3\ (\text{gas}) + 2HF\ (\text{gas})$$

In the first step, as illustrated in Fig. 1(a), the wafer is placed on a temperature-controlled cold susceptor maintained at approximately 35 °C. A remote low-energy plasma is ignited to activate the reaction between NF_3 and NH_3, producing reactive ammonium fluoride species (NH_4F and $NH_4F{\cdot}HF$). Subsequently, these fluorinated intermediates are transported to the wafer surface, where they selectively react with SiO_2 to form the solid byproduct $(NH_4)_2SiF_6$.

In the final step, as shown in Fig. 1(b), the wafer is lifted toward the heated showerhead region, where the temperature is increased to approximately 180 °C. At this elevated temperature, the deposited $(NH_4)_2SiF_6$ undergoes thermal decomposition, releasing volatile SiF_4, NH_3, and HF species. These gaseous byproducts are evacuated from the process chamber, leaving a clean silicon surface for downstream fabrication processes.

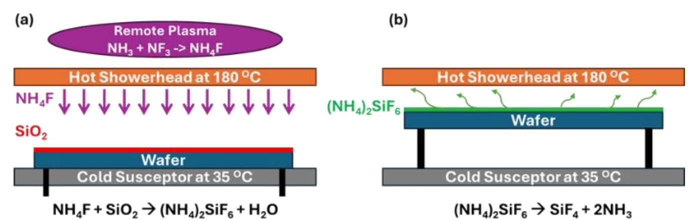

Fig. 1. Working principle of SiCoNi process. (a) Reactive species NH_4F generated by remote plasma selectively etch SiO_2 layer on wafer surface. (b) Wafer is moved closer to the heated showerhead to thermally sublimate and remove the byproducts.

Defect characterization was carried out using standard tools such as an inline laser scanning defect inspection system, scanning electron microscopy (SEM), energy dispersive X-ray spectroscopy (EDX), and transmission electron microscopy (TEM).

III. Results and Discussion

Through a systematic process partition check, hexagonal defects were first observed immediately after the ex-situ SiCoNi clean, before emitter deposition. These defects persist after the subsequent emitter deposition layer. It is further confirmed that the defects originate from the ex-situ SiCoNi process, as no similar defects are observed when this cleaning step is purposely skipped. As shown in Fig. 2(b), a gross wafer map reveals a high density of defects distributed across the wafer, with the total defect count exceeding 10,000. Such a high defect density not only adversely affects subsequent deposition and etch processes but also obscures other potential killer defects at this process layer. A representative defect image obtained under high-magnification SEM inspection is presented in Fig. 2(c). The defect exhibits a distinct hexagonal morphology with well-defined faceted edges. This indicates a crystalline nature rather than random particle contamination, which typically exhibits irregular shapes. The characteristic defect size is approximately 1 µm, which is significantly larger than the critical dimension of a 40 nm device.

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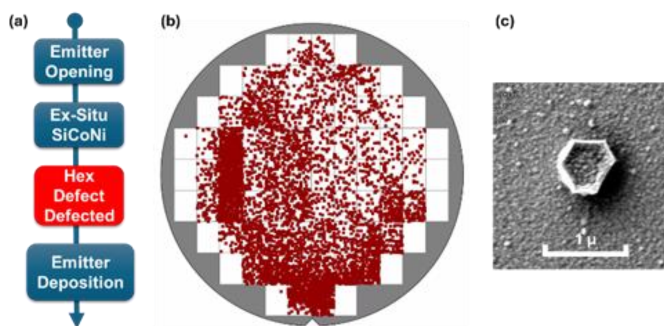

Fig. 2. (a) Hexagonal defects are first observed after ex-situ SiCoNi clean and prior to emitter deposition. (b) Inline scan reveals a gross defect map with defect counts exceeding 10,000. (c) Top view SEM image of a typical hexagonal defect.

Further investigation using high-magnification SEM and associated EDX analysis provides deeper insight into the nature of the hexagonal defects. Fig. 3(a) shows a typical top-view SEM image of a defect lying flat on the wafer surface. More importantly, a partially embedded hexagonal defect is presented in Fig. 3(b). One portion of this defect is buried inside the film, while the remaining portion protrudes above the surface. This morphology strongly suggests that the defect is not a foreign particle deposited onto the wafer surface, but rather a structure that nucleates and grows from the underlying silicon nitride spacer layer. This observation also explains why the implementation of additional scrubber cleaning or wet chemical cleaning after the SiCoNi process fails to remove the defects. Since the defects are mechanically anchored within the underlying spacer layer, they cannot be simply eliminated by surface-level cleaning processes alone. Elemental analysis performed by SEM-EDX, as shown in Fig. 3(c), reveals the presence of only three elements: Si, O, and Ge. The Ge signal is relatively weak and is likely attributed to the background contributions from the underlying SiGe base layer. In contrast, Si and O exhibit stronger signals, suggesting that the hexagonal defect is a primarily silicon oxide-based crystalline structure.

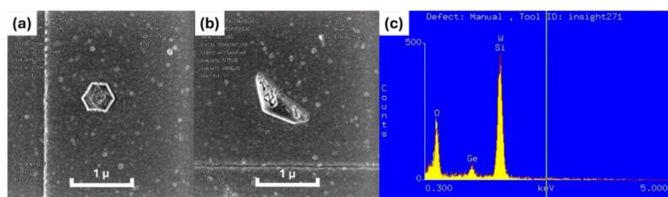

Fig. 3. Top view SEM images show a hexagonal defect (a) lying flat on the wafer surface or (b) partially embedded in the film. (c) EDX spectrum detects only Si, O and Ge elements, indicating the hexagonal defect is SiO_2 in nature.

Detailed characterization of the hexagonal defect was performed using cross-sectional TEM combined with EDX elemental mapping, as shown in Fig. 4. As revealed in Fig. 4(a), the defect exhibits a hollow structure rather than a solid morphology, with a clear void present inside the particle. This hollow nature further suggests that the defect is formed in situ rather than originating from flaking quartzware fragments from the equipment. EDX elemental mapping was performed for four elements: Si, O, N, and Ge, as shown in Fig. 4(b)-(e), where different colors represent the spatial distribution of each element. The EDX mapping results clearly indicate that the defect region contains only Si and O, with no detectable nitrogen signal within the defect. The Ge signal is attributed to the underlaying SiGe base layer and does not overlap with the defect region. These observations are consistent with the SEM-EDX results discussed earlier, confirming that the hexagonal defect is composed of silicon oxide. With the defect composition unambiguously identified, the next critical question is the origin of this silicon oxide formation during the ex-situ SiCoNi process.

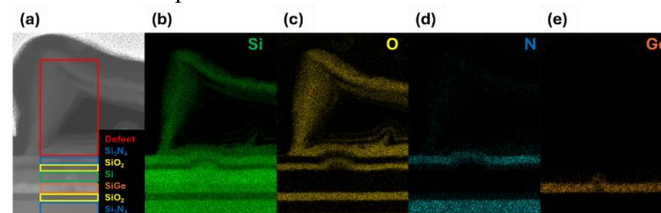

Fig. 4. (a) Cross-sectional TEM image of hexagonal defect reveals a hollow structure. EDX elemental mappings of (b) silicon (c) oxygen (d) nitrogen (e) germanium. The EDX mappings confirm that the hexagonal defect is SiO_2 in nature, where the Ge signal is from the buried SiGe base layer.

A common concern for particle-related issues is whether the observed defects originate from the equipment hardware, such as coating delamination or quartzware flaking. To rule out the possibility that the hexagonal defects are tool-specific, patterned wafers were processed using three different ex-situ SiCoNi tools. All tools consistently exhibited hexagonal defects with comparable defect density levels, indicating that the phenomenon is not associated with a specific process chamber. In addition, particle baseline verification was performed using blanket test wafers to assess the cleanliness of the SiCoNi tools. A silicon dioxide film was first deposited on bare silicon wafers using an LPCVD process with TEOS as the precursor. Film thickness was measured by ellipsometry to calibrate the etch rate, followed by particle inspection using a laser scanning tool to evaluate particle counts before and after the SiCoNi process. The corresponding pre- and post-process wafer maps are shown in Fig. 5. As observed, the wafer maps remain quite clean after the SiCoNi process, with comparable particle counts before and after processing. This result confirms that the SiCoNi tools exhibit good particle baseline performance and do not contribute to the gross defect maps observed on patterned wafers. Therefore, the origin of the hexagonal defects cannot be attributed to tool hardware alone. Instead, defect formation must involve interactions between the production device structure and the process conditions.

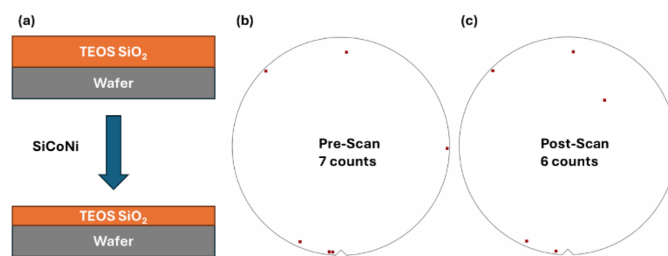

Fig. 5. (a) Film stack of test wafer used for SiCoNi particle monitoring. Inline laser scan map of test wafer (b) before and (c) after SiCoNi process, showing comparable defect counts.

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To understand why the hexagonal defects are observed only on patterned wafers rather than blanket test wafers, the schematic film stack of the patterned wafer is illustrated in Fig. 6(a). For clarity, only the outermost layers on the wafer frontside and backside are shown. As discussed previously in Fig. 4(a), the outermost layer on the wafer frontside is the silicon nitride spacer. Due to the specific device design, the emitter opening window occupies only a small fraction of the wafer surface, while most of the surface area is covered by silicon nitride. Fig. 6(b) shows a cross-sectional TEM image of the patterned wafer backside. In contrast to the frontside, the outermost layer on the backside is silicon oxide. This asymmetry between the frontside and backside surface materials originates from the fabrication process flow and equipment used. For instance, the nitride spacer is deposited using an LPCVD chamber in which film deposition occurs only on the wafer frontside. Compared to the blanket wafer shown in Fig. 5(a), both the frontside and backside surface materials of the patterned wafers are fundamentally different. Notably, the hexagonal defects are observed exclusively on the frontside silicon nitride region. This phenomenon cannot be simply attributed to the larger surface coverage of the silicon nitride layer. Instead, it suggests that this specific layer plays a critical role in the formation of the hexagonal defects.

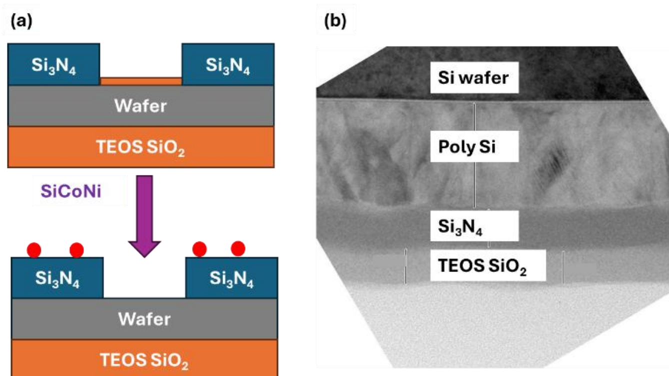
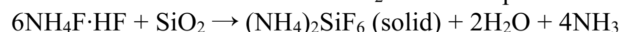


Fig. 6. (a) Schematic of the outermost layer of a patterned wafer at the SiCoNi process step, with wafer frontside of Si_3N_4 and wafer backside TEOS based SiO_2. (b) Cross sectional TEM reveals the patterned wafer backside film stack, showing the outermost layer is TEOS based SiO_2.

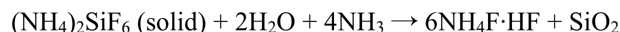
We hypothesize that the hexagonal defects originate from the reaction between residual intermediate byproducts, specifically $(NH_4)_2SiF_6$, and absorbed water moisture, leading to the formation of crystalline silicon oxide. This process can be regarded as the reverse reaction of the low-temperature silicon oxide etching process in the SiCoNi chamber, suggesting that the overall reaction pathway is partially reversible. As discussed previously and reported in multiple studies, incomplete sublimation and removal of the $(NH_4)_2SiF_6$ byproduct is a known challenge in the SiCoNi process. For the device investigated in this work, the silicon nitride spacer is deposited by a low-temperature LPCVD process, which is known to result in a porous microstructure. This porous film can facilitate the retention of SiCoNi reaction byproducts. Once trapped inside, the residual $(NH_4)_2SiF_6$ can subsequently react with ambient water moisture, leading to localized re-oxidation and the formation of silicon dioxide. This proposed mechanism is consistent with the observed partially embedded morphology of the hexagonal defects, in which the particle is anchored within the silicon nitride spacer and protrudes above the surface.

Selective chemical reaction with SiO_2 at low temperature:



$$6NH_4F\cdot HF + SiO_2 \rightarrow (NH_4)_2SiF_6\ (solid) + 2H_2O + 4NH_3$$

Reverse reaction leading to silicon dioxide hexagonal defect formation:



$$(NH_4)_2SiF_6\ (solid) + 2H_2O + 4NH_3 \rightarrow 6NH_4F\cdot HF + SiO_2$$

To validate the proposed hypothesis, two designs of experiments (DOEs) were conducted to address the two key reaction species involved in the defect formation mechanism. The first DOE focuses on mitigating the incomplete sublimation of the fluorosilicate byproduct $(NH_4)_2SiF_6$. As reported in previous studies, multi-step SiCoNi processes or more aggressive baking conditions have been demonstrated to enhance the removal of fluorosilicate salts from the wafer surface [7], [10]. Similar approaches were therefore evaluated in this work. In the first experiment, a multi-cycle etch-sublimation SiCoNi process was implemented. The total etch duration was kept constant to ensure the same amount of surface silicon oxide removal. The total thermal sublimation duration was extended from 100 s to 300 s, and the showerhead temperature was increased from 180 °C to the hardware maximum of 200 °C. As shown in Fig. 7(a), the defect density is reduced compared to the baseline process. The wafer edge region becomes defect-free, while the wafer center region still exhibits a gross defect map with high defect density. This result indicates that the enhanced SiCoNi process can partially improve the removal of residual byproducts. However, its overall effectiveness remains limited by the maximum achievable hardware temperature.

In contrast, when an additional rapid thermal anneal (RTA) process at 800 °C for 60 s was inserted before the ex-situ SiCoNi clean, the hexagonal defects were eliminated. This anneal densifies the low-temperature deposited porous silicon nitride film, thereby preventing the trapping of residual fluorosilicate byproducts generated by the SiCoNi process. The observed hexagonal defects are associated with the specific low temperature silicon nitride film employed in the device fabrication flow, which explains why similar defects have not been reported in prior studies. As shown in Fig. 7(b), the wafer with annealing remains clean even at downstream inspection. Although the high-temperature RTA resolves the SiCoNi-induced defect issue, the additional thermal budget introduced is not compatible with the existing device integration scheme. Therefore, an alternative mitigation strategy is required to address the potential moisture source involved in the reverse reaction.

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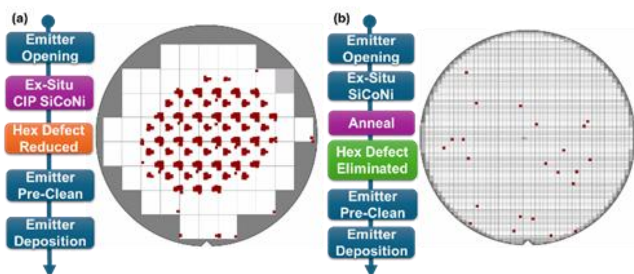

Fig. 7. (a) Ex-situ SiCoNi with multiple etch-sublimation cycles, extended sublimation duration and higher temperature eliminates hexagonal defects at wafer edge, but defects persist at wafer center. (b) Inserting an 800 °C, 60 s RTA step before SiCoNi process fully eliminates hexagonal defects.

An interesting phenomenon is observed when every wafer in a slot is inspected immediately after the ex-situ SiCoNi process. As illustrated in Fig. 8, the wafer placed at the topmost position inside the FOUP is consistently clean, with no hexagonal defects observed, despite all wafers undergoing identical process conditions. The SiCoNi process is a single-wafer chamber process in which wafers are processed sequentially from slot 1 (bottommost) to slot 25 (topmost) of the FOUP. Therefore, the observed phenomenon cannot be attributed to a first-wafer effect. Furthermore, even when only a limited number of wafers are loaded inside the FOUP, the wafer located at the relative topmost position also remains clean. In addition, even though the two wafers were loaded sparsely separated by multiple empty slots, the hexagonal defect is only observed on the bottom wafer. These observations indicate a strong dependence of hexagonal defect formation on FOUP slot position. Notably, the only difference for the topmost wafer compared to other wafers inside the FOUP is that its frontside is not facing the backside of another wafer. This strongly suggests that the backside condition of patterned wafers plays a critical role in the formation of hexagonal defects.

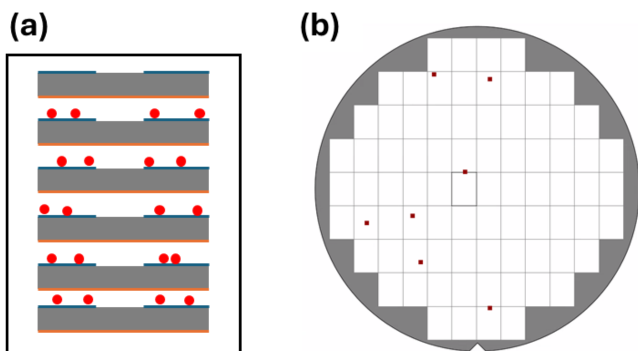

Fig. 8. (a) Hex defects are not observed on the wafer placed at the topmost slot of the FOUP. (b) Inline scan defect map of the topmost wafer shows a clean surface.

To further validate the proposed hypothesis, a second experiment was conducted to remove the wafer backside TEOS silicon oxide layer. As illustrated in Fig. 9(a), a backside TEOS removal step was introduced prior to the emitter opening and the ex-situ SiCoNi process. The cross-sectional TEM image in Fig. 9(b) confirms this modification, showing that silicon nitride becomes the outermost layer on the wafer backside. The wafers subsequently underwent the standard ex-situ SiCoNi process. As shown in Fig. 9(c), the resulting wafer defect map is clean, with no hexagonal defects observed. The TEOS silicon oxide film was originally deposited in an LPCVD furnace at a relatively low temperature of ~600 °C, without any subsequent high-temperature densification due to thermal budget constraints. As a result, this film is porous and contains residual silanol (Si-OH) groups. This leads to poor resistance to moisture and facilitates the absorption of water molecules during wet cleaning processes [29], [30]. When wafers are stored inside the FOUP, the absorbed moisture can desorb from the backside TEOS film and migrate towards the frontside of the wafer below, where it reacts with trapped $(NH_4)_2SiF_6$. This desorption process is time-dependent and influenced by fab environment, with hexagonal defects observed only after storage times exceeding 9.5 hours in our study. As a result, silicon oxide hexagonal defects are formed inside the silicon nitride spacer. By removing the backside TEOS film, this moisture source is effectively eliminated. Although residual $(NH_4)_2SiF_6$ byproducts may still exist within the silicon nitride spacer, the absence of water moisture prevents the reverse reaction from occurring, thereby suppressing the formation of silicon oxide hexagonal defects.

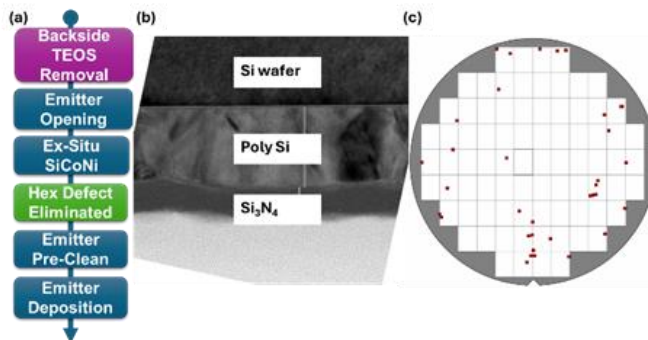

Fig. 9. (a) Process flow illustrating insertion of a backside TEOS oxide removal step prior to emitter opening. (b) Cross sectional TEM image of wafer backside film stack after process flow modification, showing Si_3N_4 as the outermost layer. (c) A clean wafer defect map is observed after ex-situ SiCoNi processing after removal of the backside TEOS film.

The proposed mechanism for SiCoNi-induced silicon oxide hexagonal defect formation is summarized in Fig. 10. To the best of our knowledge, this specific defect phenomenon has not been previously reported. This is likely attributed to the unique combination of porous silicon nitride spacers and TEOS-based silicon oxide employed in the patterned wafers investigated in this study. In addition, the stringent thermal budget constraints required for the 40 nm BiCMOS device further reduce the process margin window. As demonstrated in this work, the formation of hexagonal defects can be effectively suppressed by eliminating either the residual $(NH_4)_2SiF_6$ byproduct or the moisture source involved in the reverse reaction pathway.

This study presents a systematic investigation of SiCoNi-induced defect formation and proposes practical mitigation strategies that are compatible with existing device integration schemes. The insights gained are not limited to the specific

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scenario discussed here but can be broadly applied to remote plasma-assisted dry clean processes used in advanced semiconductor manufacturing.

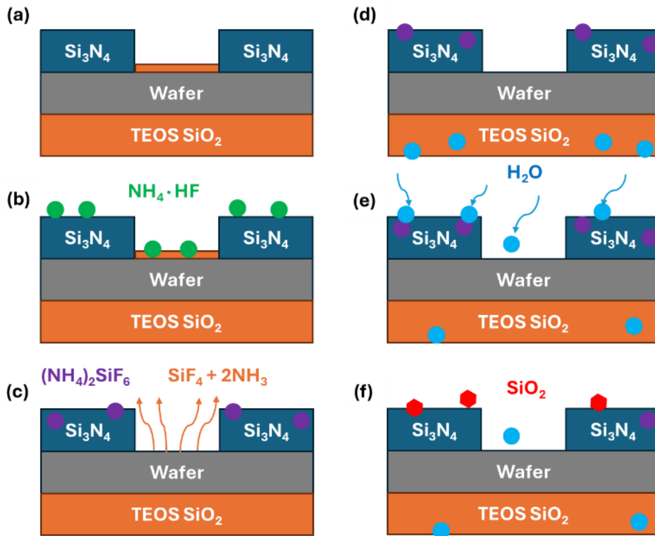

Fig. 10. Proposed mechanism for SiCoNi-induced hexagonal defect formation. (a) Initial wafer stack prior to SiCoNi treatment. (b) Remote plasma generates $NH_4{\cdot}HF$, which adsorbs on the wafer frontside. (c) $NH_4{\cdot}HF$ reacts selectively with SiO_2, releasing SiF_4 and NH_3 that readily sublimate. In contrast, byproduct $(NH_4)_2SiF_6$ is trapped inside Si_3N_4 spacer film. (d) H_2O molecules from wet cleaning process subsequently absorb and accumulate within the porous TEOS based SiO_2 on the wafer backside. (e) During wafer storage inside the FOUP, the absorbed moisture gradually diffuses outward from the TEOS layer and re-adsorbs onto the wafer frontside. (f) The arriving H_2O reacts with the trapped $(NH_4)_2SiF_6$ within the Si_3N_4 region, leading to localized SiO_2 crystallite formation, which manifests as the observed hexagonal defects.

IV. Conclusion

In this work, a systematic investigation was conducted to identify the root cause and formation mechanism of SiCoNi-induced silicon oxide hexagonal defects observed at the pre-clean step of the NPN-emitter layer in a 40 nm BiCMOS device. Design-of-experiments results demonstrated that fluorosilicate byproducts, $(NH_4)_2SiF_6$, generated from the SiCoNi process can be trapped inside the porous silicon nitride spacer layer on the wafer frontside. Water moisture originating from ambient exposure or wet cleaning processes can be absorbed and retained in the TEOS-based silicon oxide layer on the wafer backside. When these two species interact inside the FOUP, a reverse reaction occurs leading to localized oxidation and the formation of crystalline silicon oxide hexagonal defects. Either inserting a high-temperature annealing step or removing the backside TEOS film can mitigate this defect issue.

This study highlights the interaction between ex-situ dry clean processes, material properties, and device fabrication flow integration. The insights and mitigation strategies proposed here are not limited to the specific device architecture or process conditions investigated but are broadly applicable to remote plasma-assisted dry clean processes in advanced semiconductor manufacturing.

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